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Claims

[c1] 1.A method of forming a high voltage metal oxide semiconductor (HVMOS) transistor comprising:
providing a substrate having a first conductive type well;
forming a polysilicon layer on the substrate;
forming a first patterned photoresist layer on the polysilicon layer, and utilizing the first patterned photoresist layer as a hard mask to remove a portion of the polysilicon layer not covered by the first patterned photoresist layer such that a gate structure is formed;
forming a second patterned photoresist layer onto the first patterned photoresist layer and the substrate such that two openings are formed alongside the gate;
utilizing the first patterned photoresist layer and the second patterned photoresist layer as a hard mask to perform at least an ion implantation process for forming a second conductive type double diffuse drain via the openings; and
removing the first patterned photoresist layer and the second patterned photoresist layer.

[c2] 2.The method of claim 1 wherein the steps of forming the first patterned photoresist layer comprises:

coating a photoresist layer on the polysilicon layer;
performing an exposure process and a development process on the photoresist layer; and
performing an ultraviolet curing process on the photoresist layer.

[c3] 3.The method of claim 1 further comprising performing an ultraviolet curing process on the first patterned photoresist layer before the second patterned photoresist layer is formed.

[c4] 4.The method of claim 1 wherein the substrate comprises two filed oxide layers.

[c5] 5.The method of claim 4 wherein the steps of forming the second patterned photoresist layer comprises:
coating a photoresist layer onto the substrate and the first patterned photoresist layer; and
removing a portion of the photoresist layer such that the patterned photoresist layer is formed on the two field oxide layers and around the gate.

[c6] 6.The method of claim 5 wherein the steps of forming the double diffuse drain is performed after forming the second patterned photoresist layer, the steps comprises:
performing a first ion implantation process;
performing a descum process to laterally remove a por-

tion of the second patterned photoresist layer such that the two openings are enlarged; and
performing a second ion implantation process.

[c7] 7.The method of claim 1 wherein the ion implantation process comprises a first ion implantation process and a second ion implantation process.

[c8] 8.The method of claim 7 wherein the doped concentration of the second ion implantation process is higher than the doped concentration of the first ion implantation process.

[c9] 9.The method of claim 7 wherein the first ion implantation process uses same dopants as the second ion implantation process.

[c10] 10.The method of claim 7 wherein the first ion implantation process uses different dopants from the second ion implantation process.

[c11] 11.A method of forming a semiconductor transistor with double diffuse drain (DDD) in a substrate, the substrate comprising a first conductive type well, the method comprising:
forming a polysilicon layer and a first photoresist layer on the substrate;
removing a portion of the first photoresist layer and per-

forming an ultraviolet curing process to the first photoresist layer;

utilizing the first photoresist layer as a hard mask to remove a portion of the polysilicon layer not covered by the first photoresist layer such that a gate structure is formed;

coating a second photoresist layer onto the substrate and the first photoresist layer, and removing the second photoresist layer above the first photoresist layer and removing a portion of the second photoresist layer alongside the gate structure such that two openings are formed;

utilizing the first photoresist layer and the second photoresist layer as a hard mask to perform a first ion implantation process for forming two second conductive type first doped regions in the well via the openings;

utilizing the first photoresist layer and the second photoresist layer as a hard mask to perform a second ion implantation process for forming two second conductive type second doped regions in upper portions of the two first doped regions via the openings; and

removing the first photoresist layer and the second photoresist layer.

[c12] 12.The method of claim 11 wherein the doped concentration of the second doped regions is higher than the

doped concentration of the first doped regions.

[c13] 13.The method of claim 11 wherein the first ion implantation process uses same dopants as the second ion implantation process.

[c14] 14.The method of claim 11 wherein the first ion implantation process uses different dopants from the second ion implantation process.